

FIG. 1

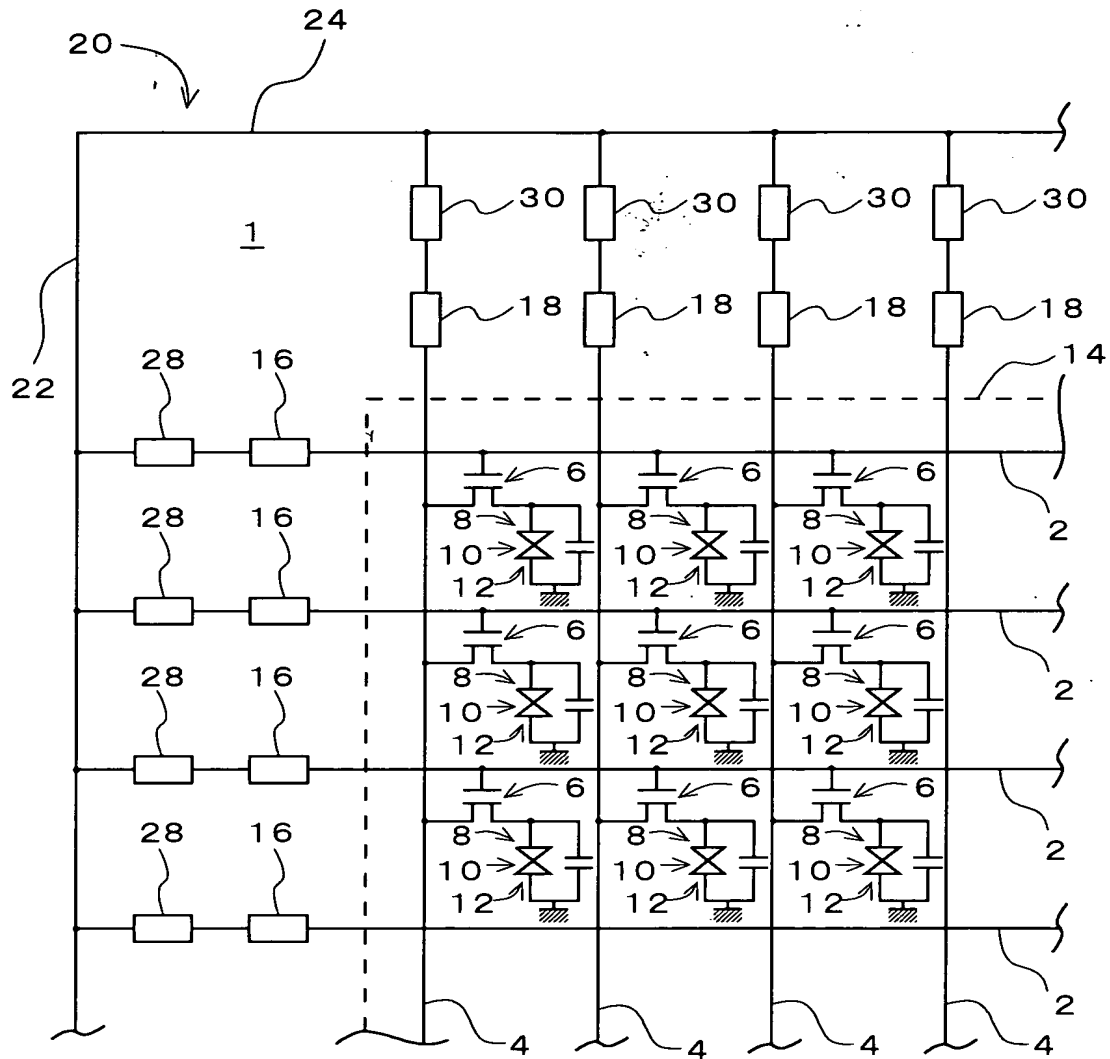


FIG. 2a

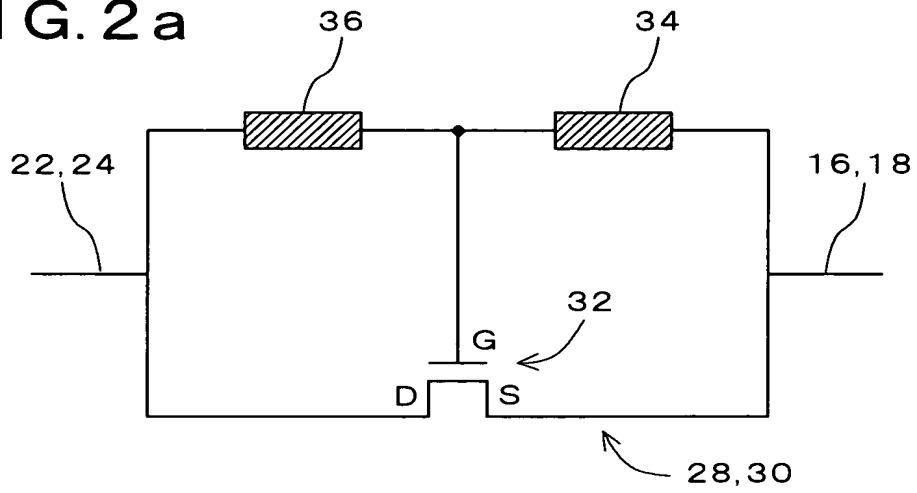


FIG. 2b

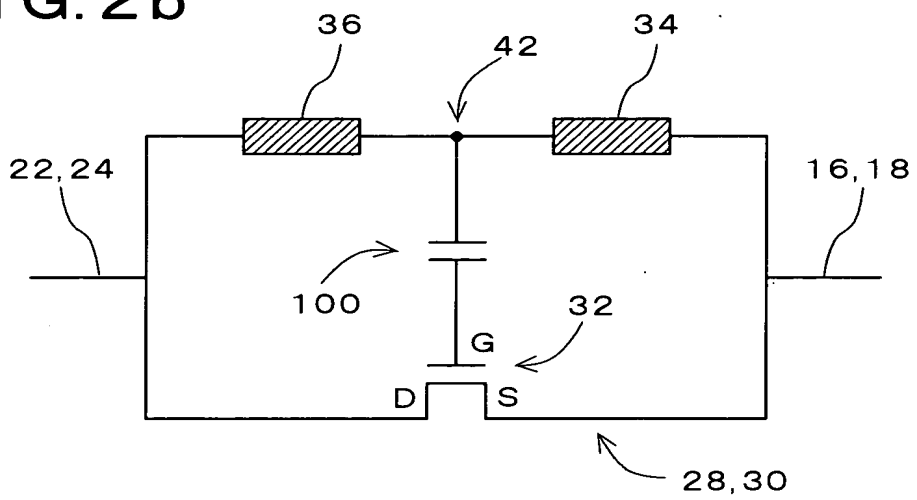


FIG. 3

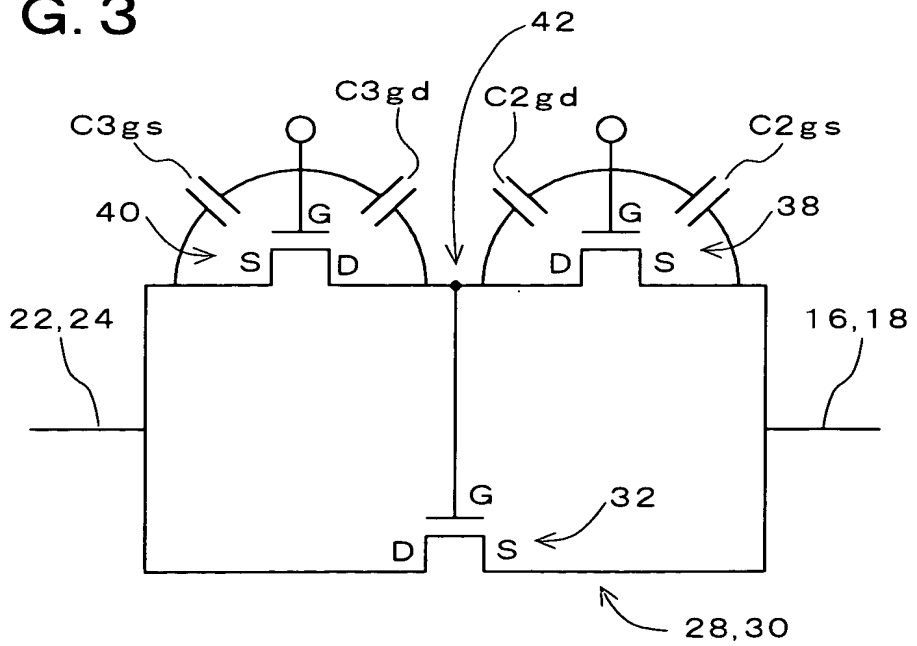


FIG. 4a

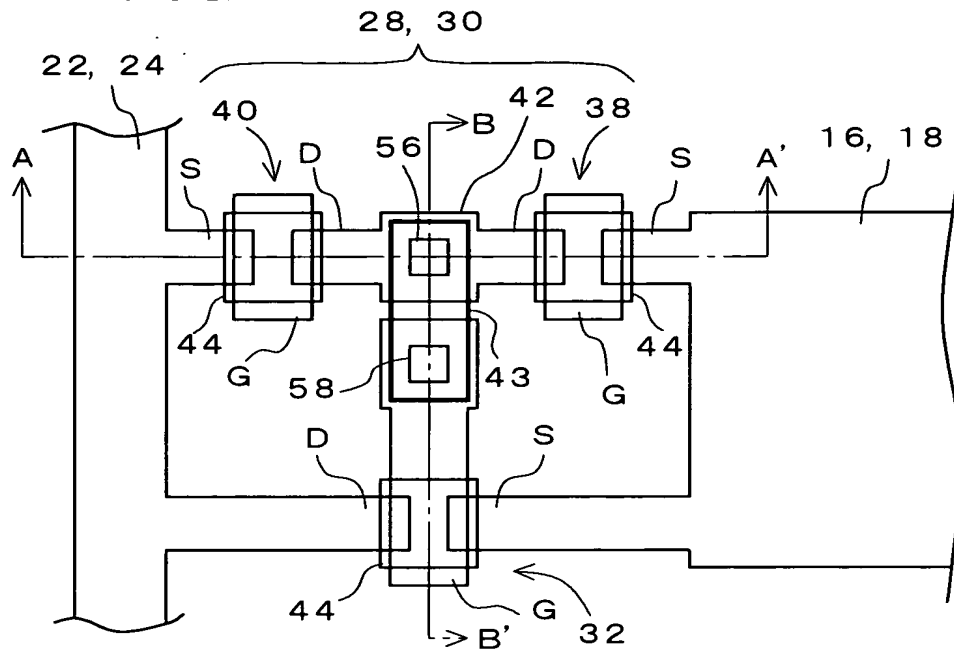


FIG. 4b

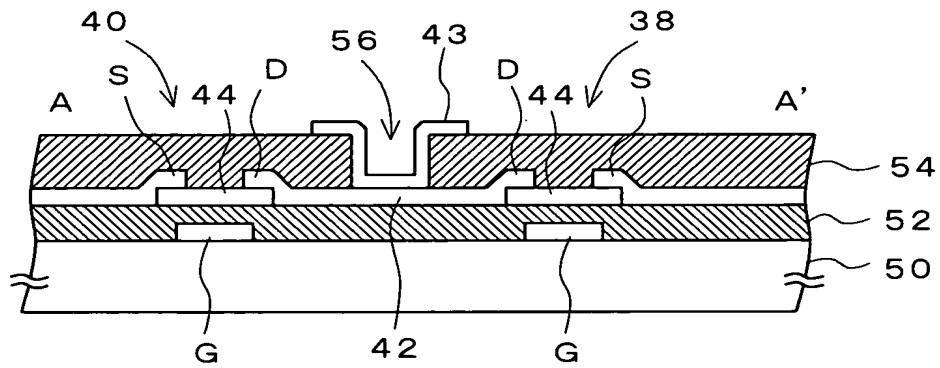


FIG. 4c

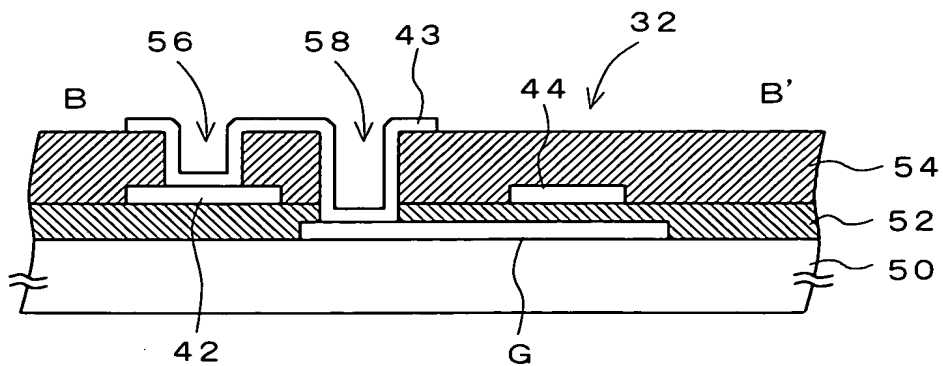


FIG. 5

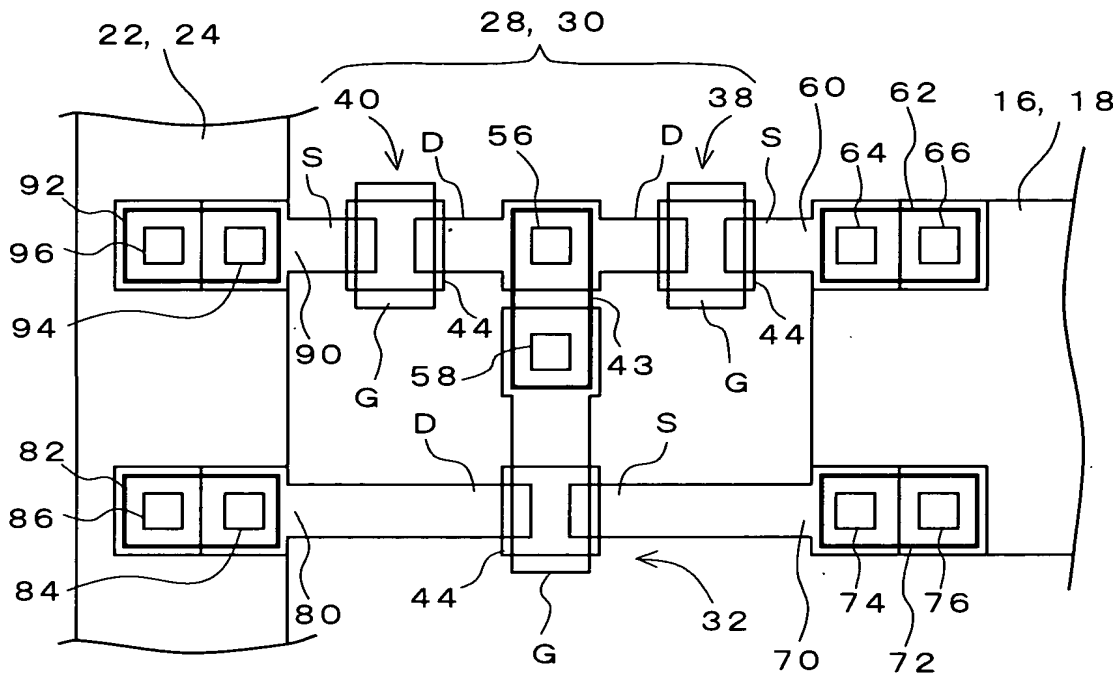


FIG. 6

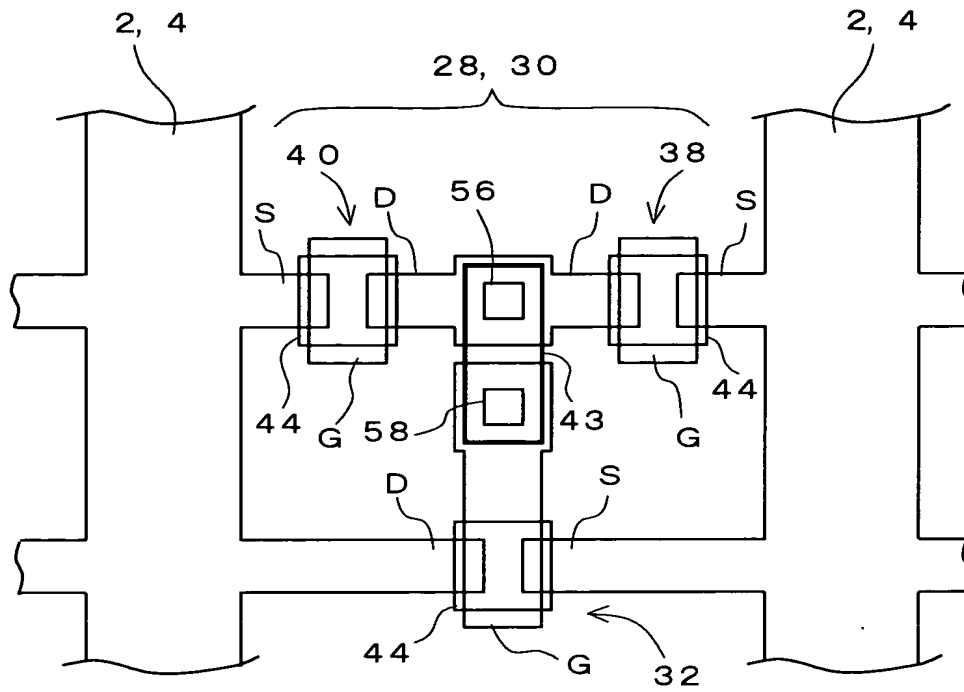


FIG. 7

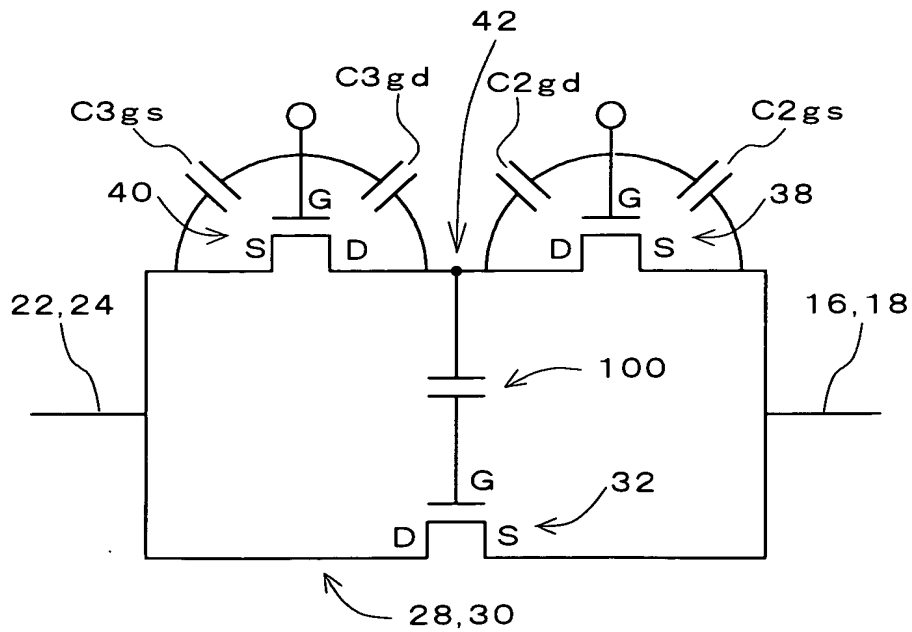


FIG. 8a

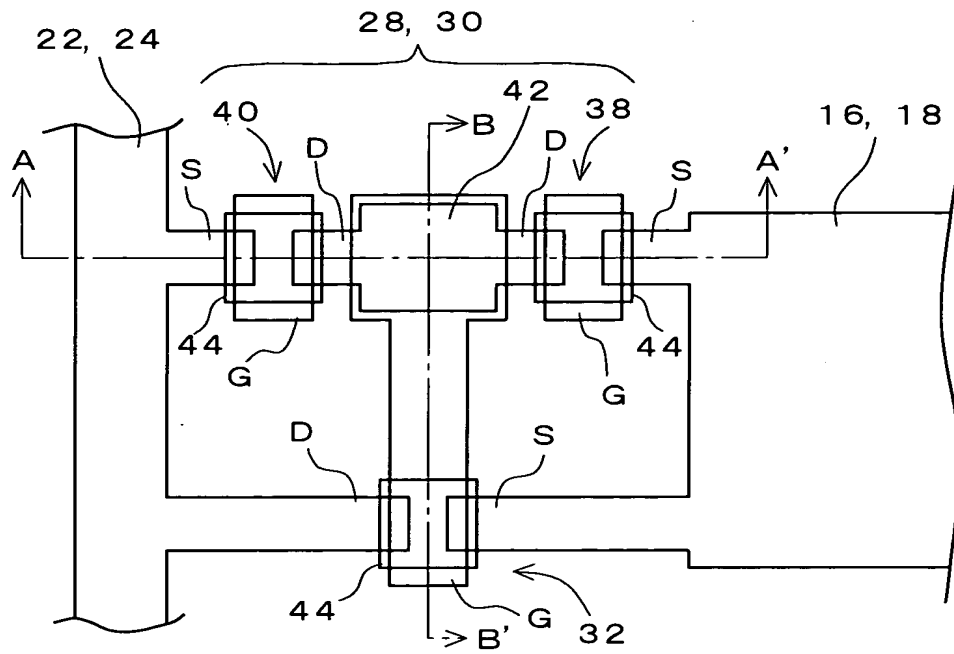


FIG. 8b

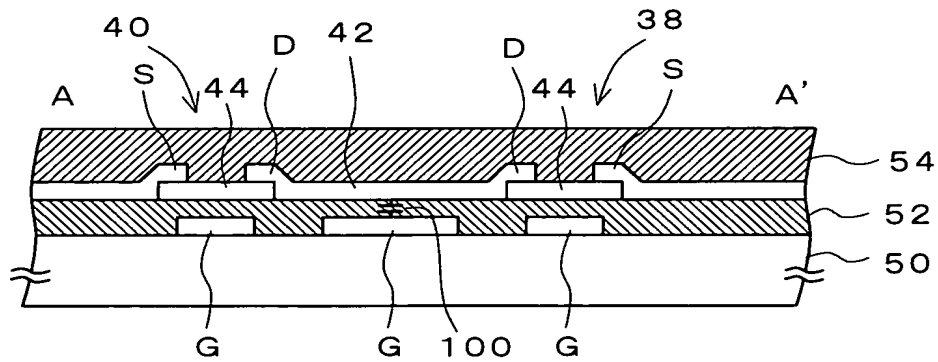


FIG. 8c

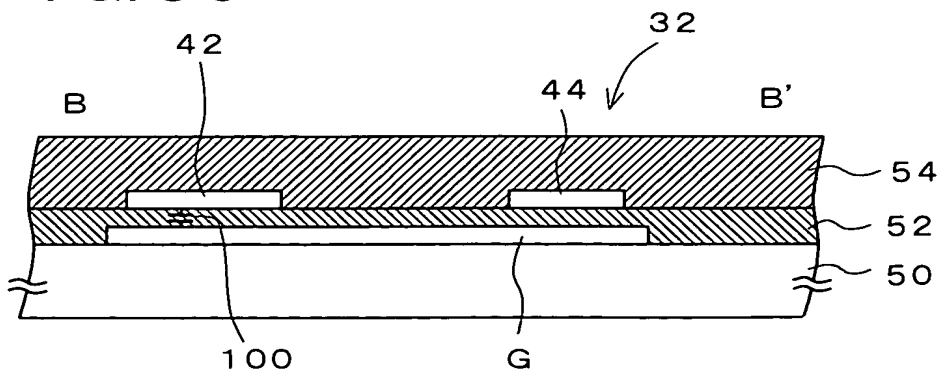
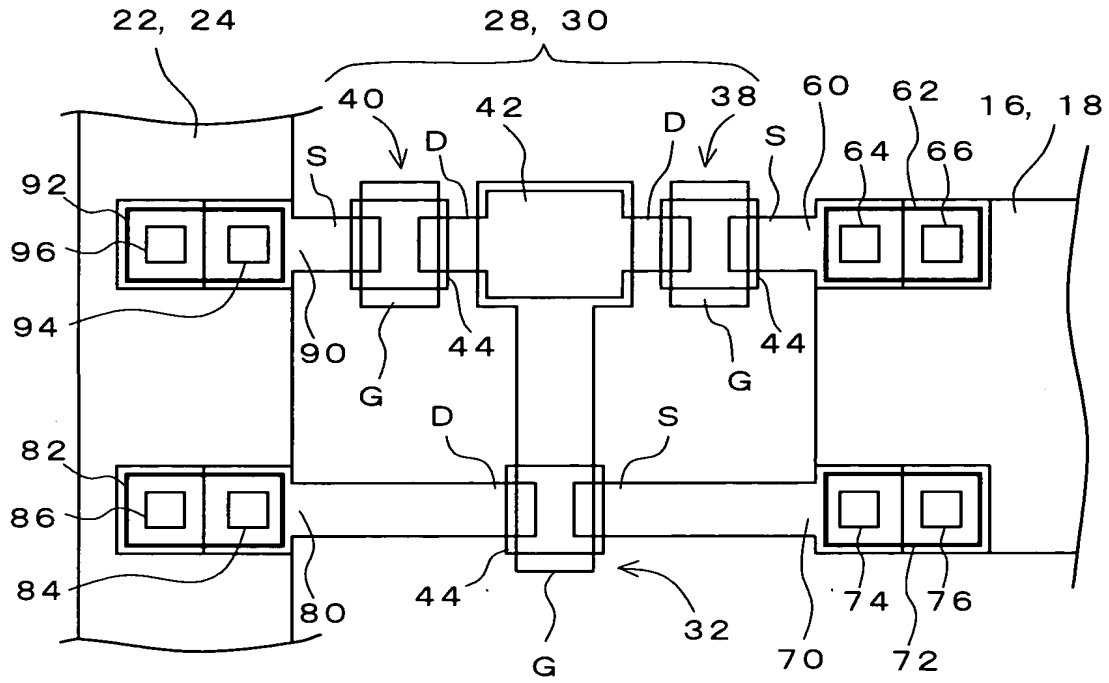
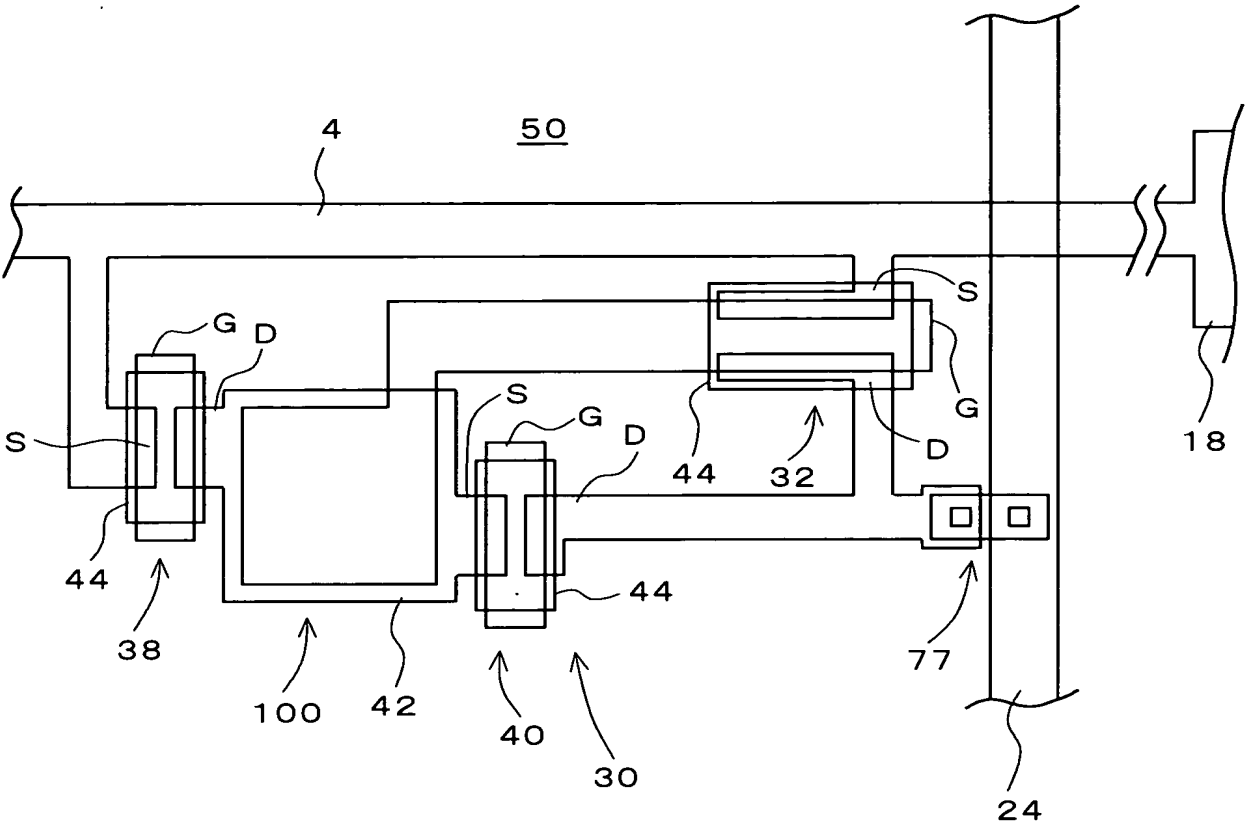


FIG. 9



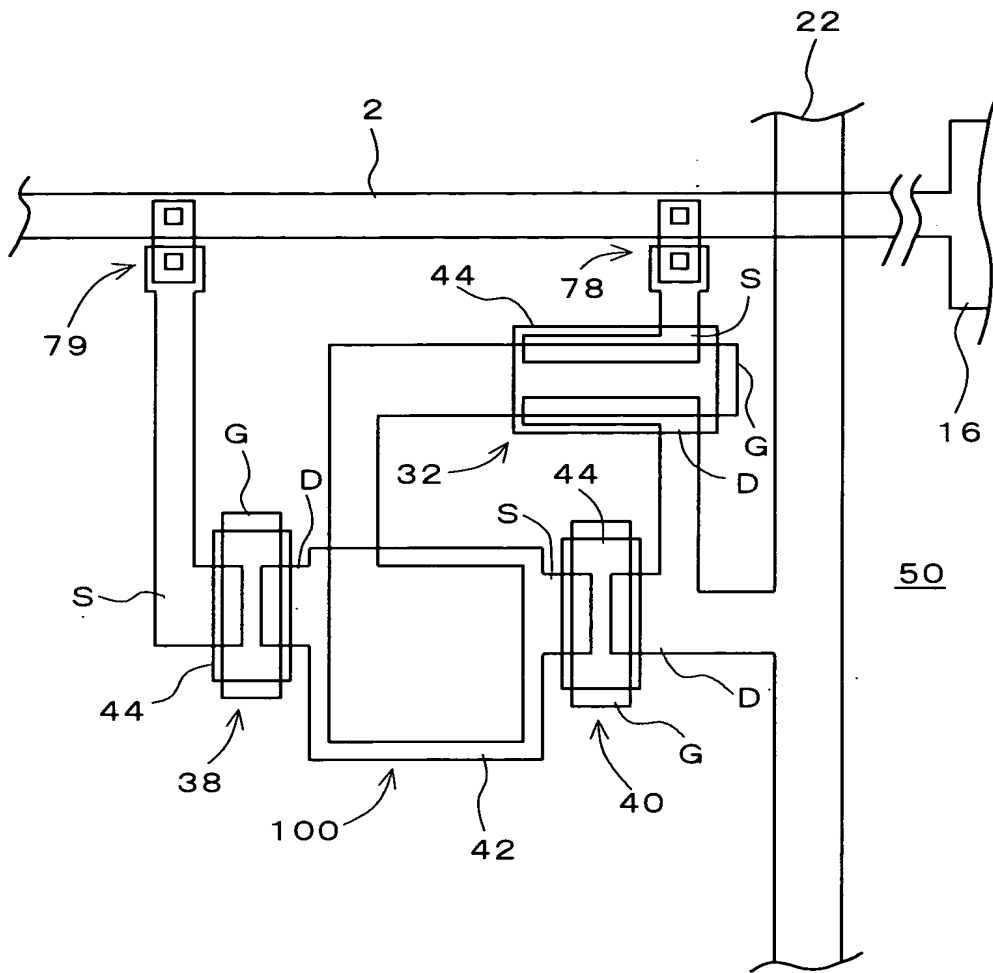
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FIG. 10



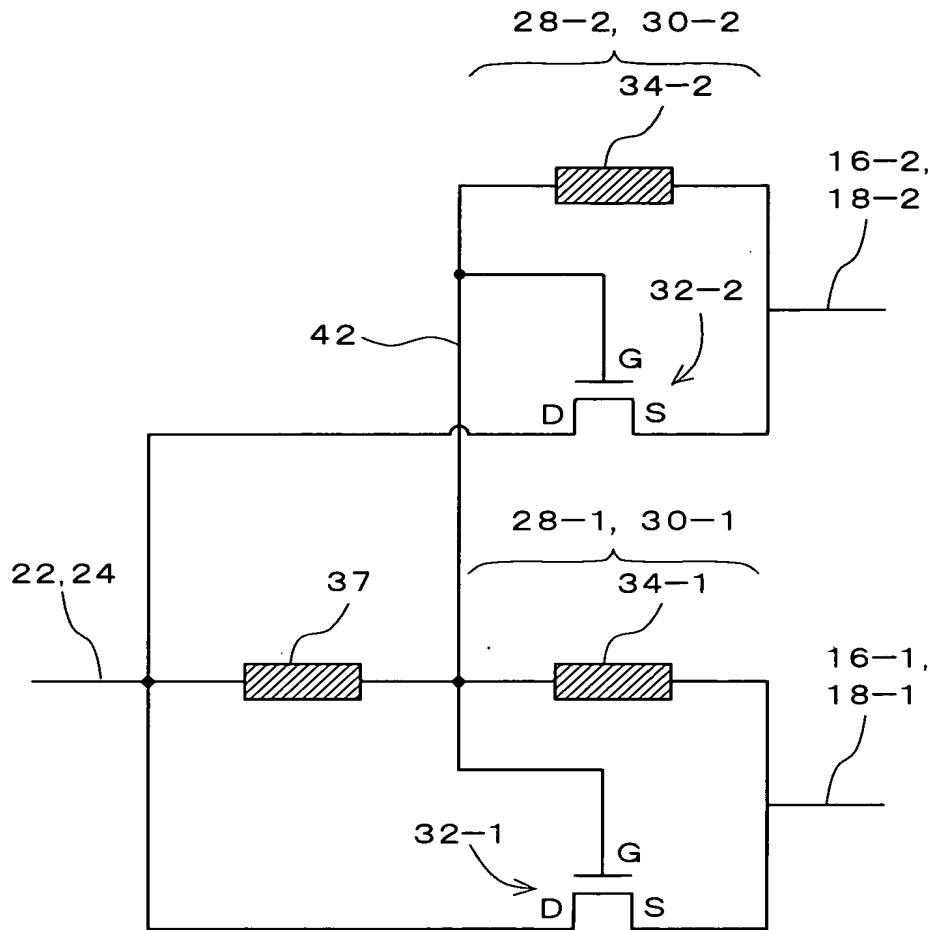
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FIG. 11



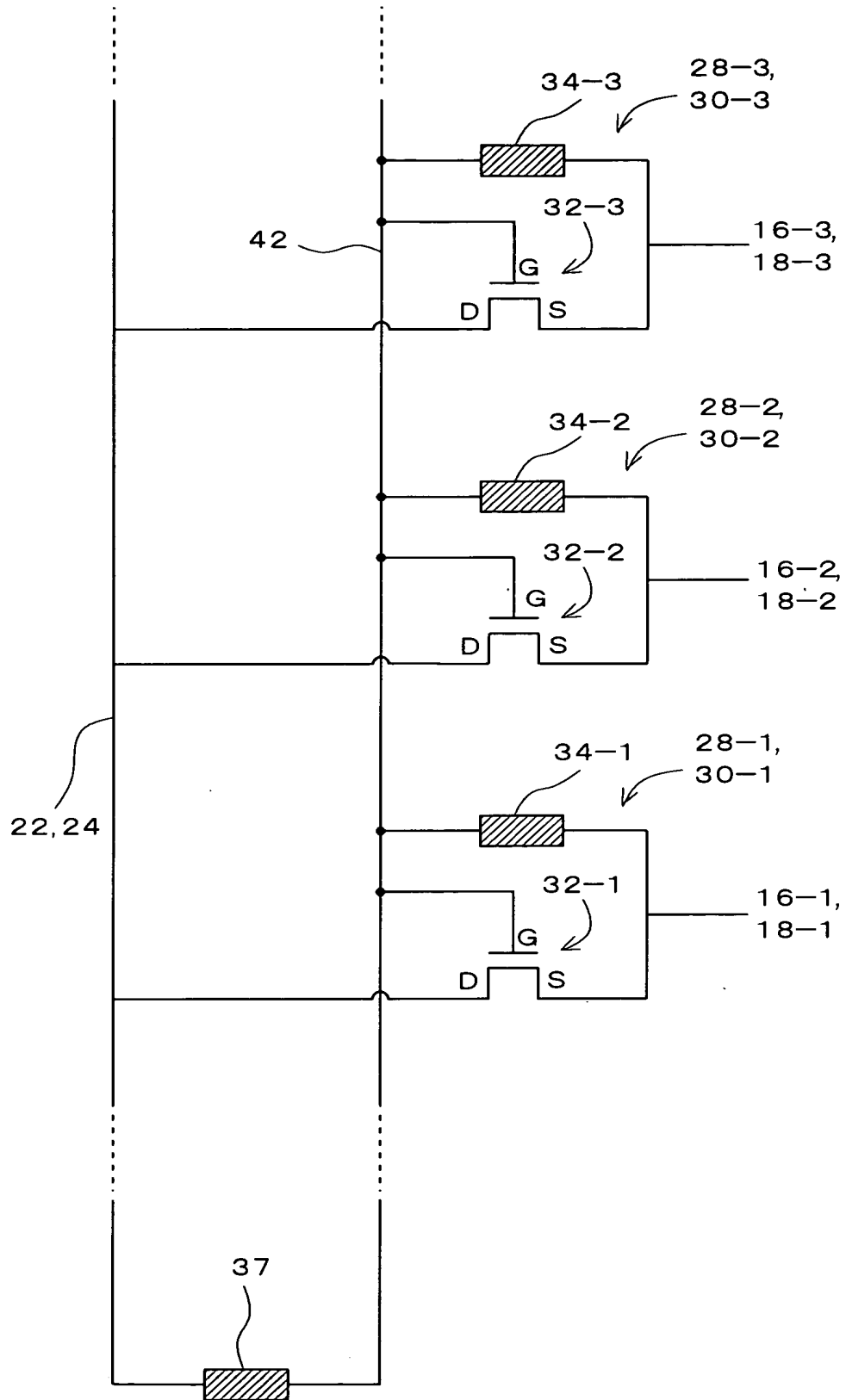
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FIG. 12



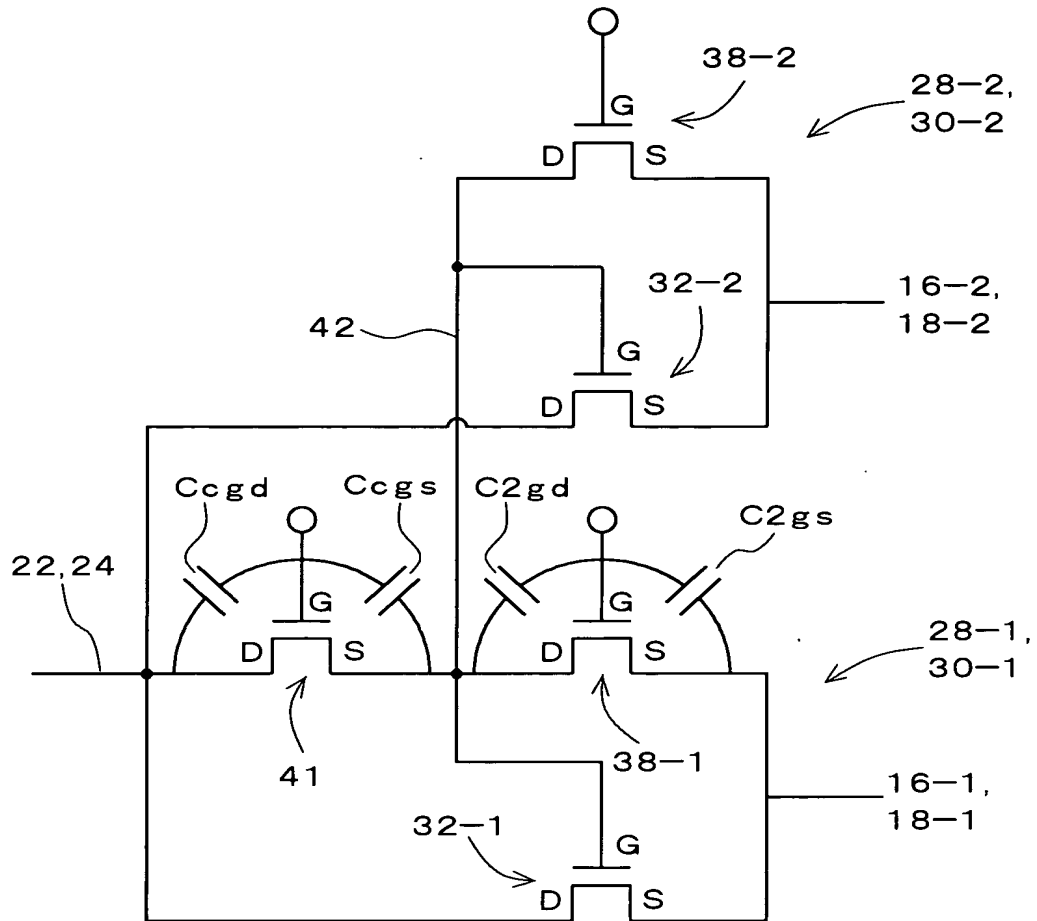
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FIG. 13



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FIG. 14



[illegible]

FIG. 16

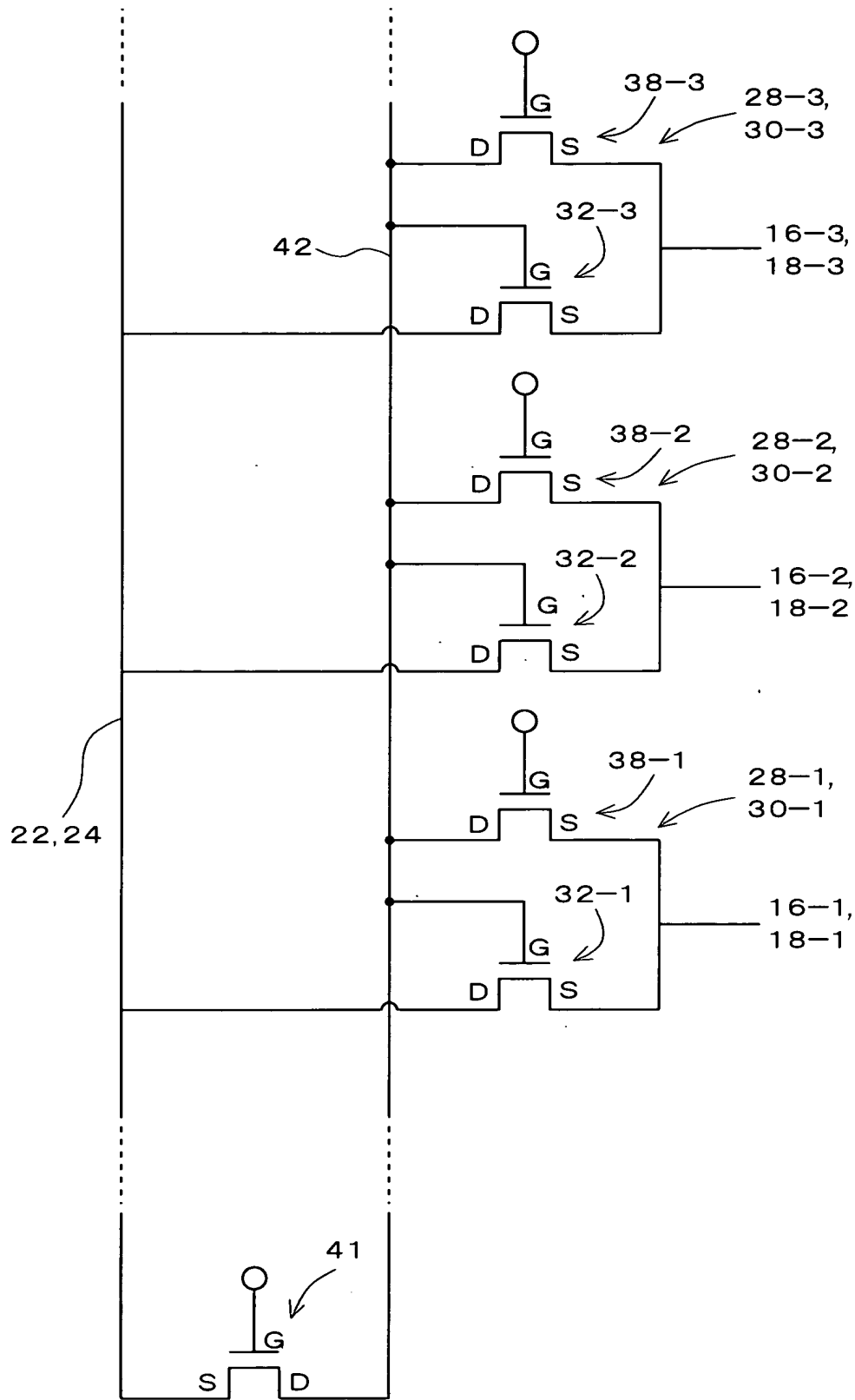
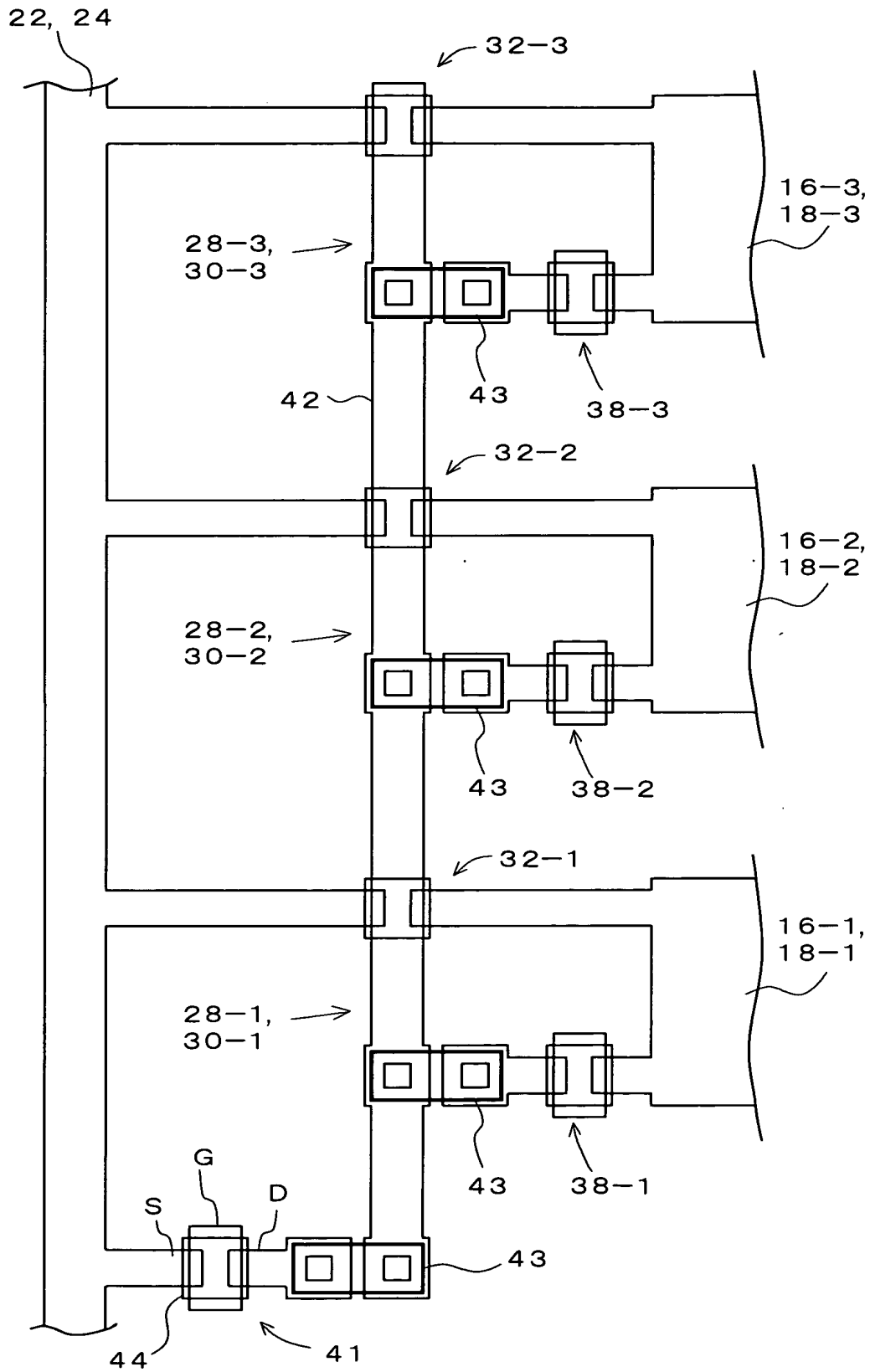


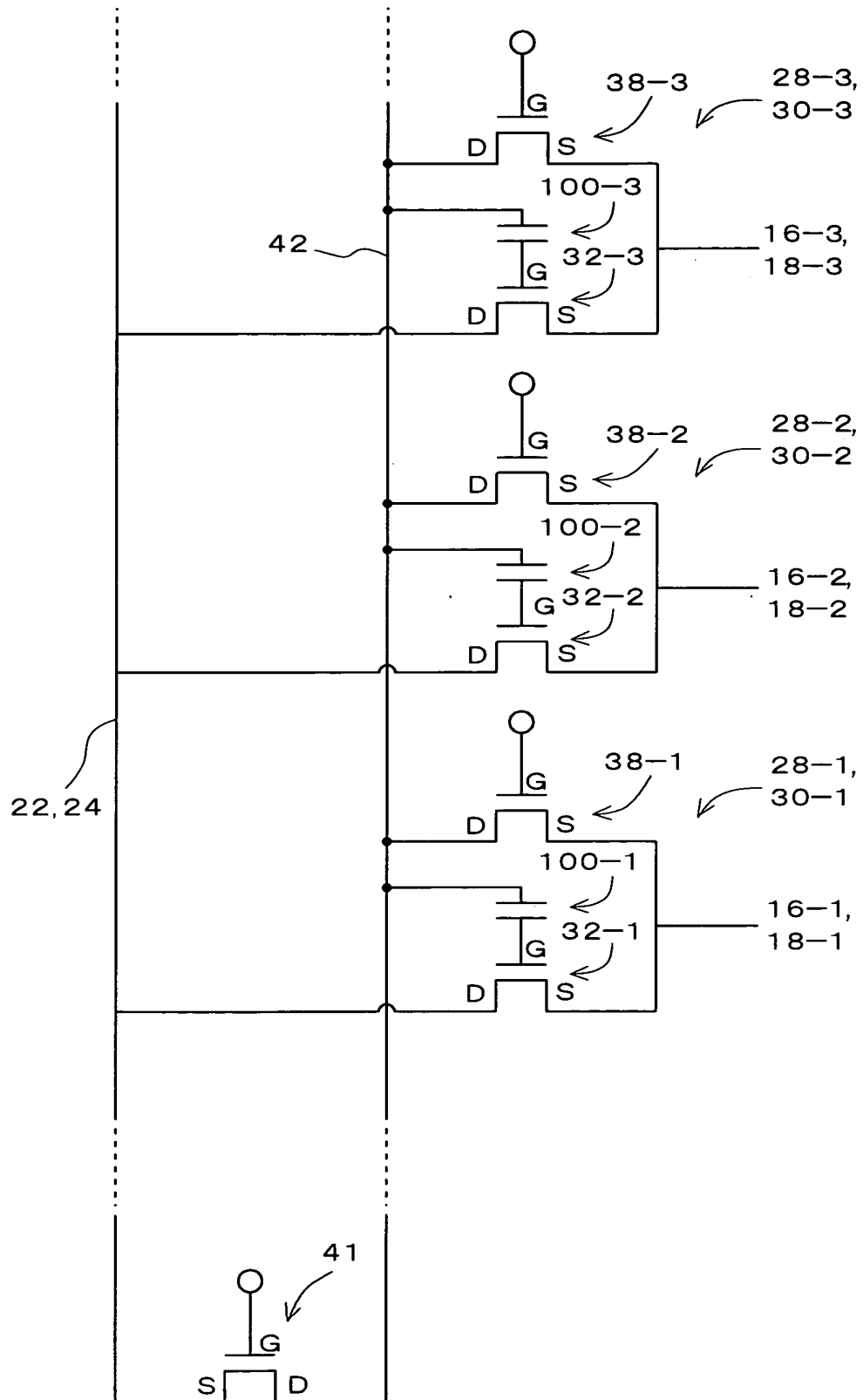
FIG. 17



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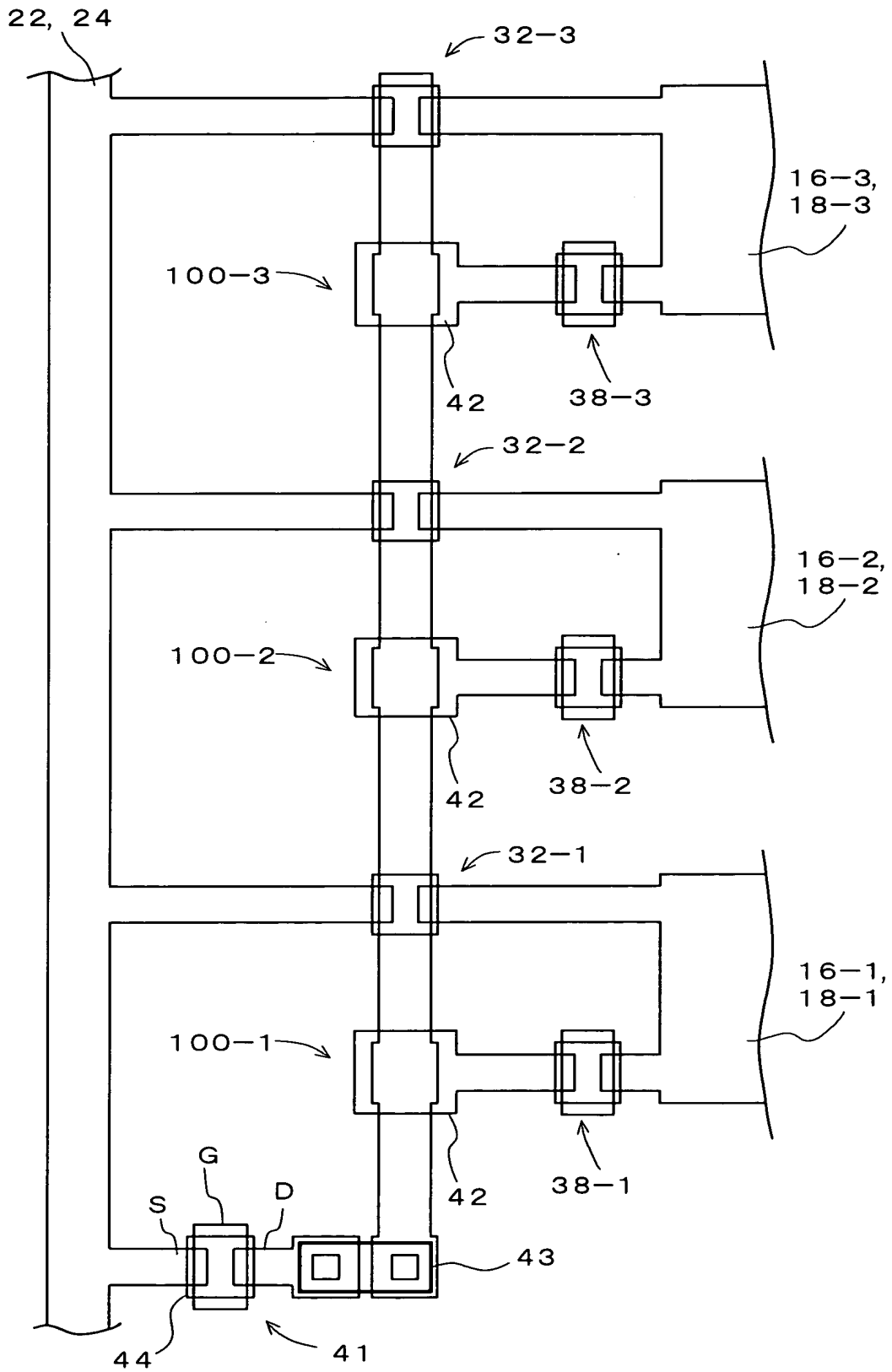
The diagram illustrates a differential signal processing circuit with two parallel branches. A common input line, labeled 22, 24, enters from the left and splits into two paths. The upper path contains a PMOS transistor 32-2 (gate 38-2, source 16-2, drain 18-2) and an NMOS transistor 32-1 (gate 38-1, source 16-1, drain 18-1). The lower path contains a PMOS transistor 32-1 (gate 38-1, source 16-1, drain 18-1) and an NMOS transistor 32-2 (gate 38-2, source 16-2, drain 18-2). The gates of the PMOS transistors are connected to a common gate line 42, and the gates of the NMOS transistors are connected to a common gate line 41. The drains of the PMOS transistors are connected to a common output node, and the drains of the NMOS transistors are connected to another common output node. The sources of the PMOS transistors are connected to a common source line, and the sources of the NMOS transistors are connected to another common source line. The gates of the PMOS transistors are also connected to a common gate line 42, and the gates of the NMOS transistors are connected to a common gate line 41.

FIG. 20



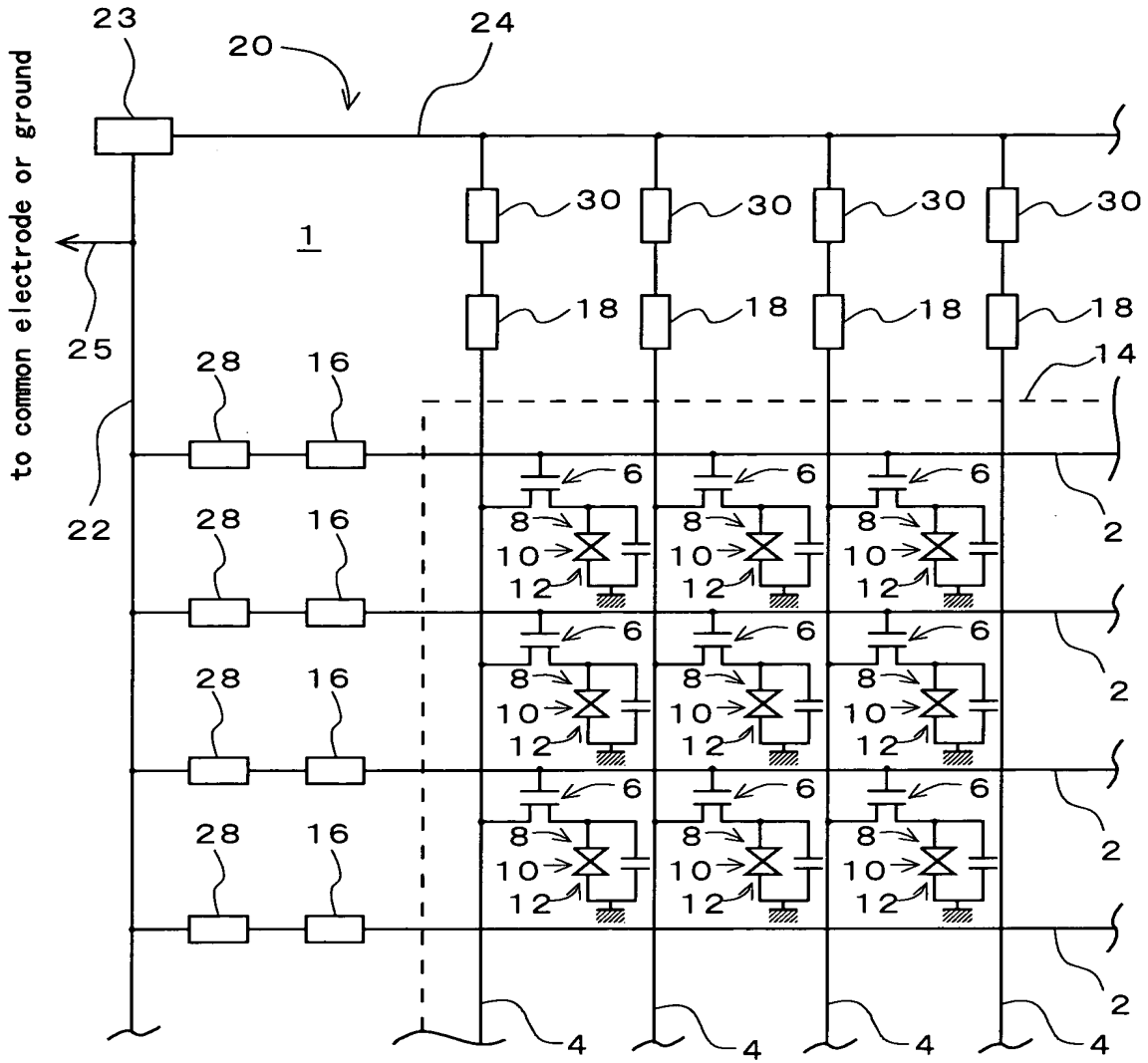
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FIG. 21



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FIG. 22



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FIG. 23a

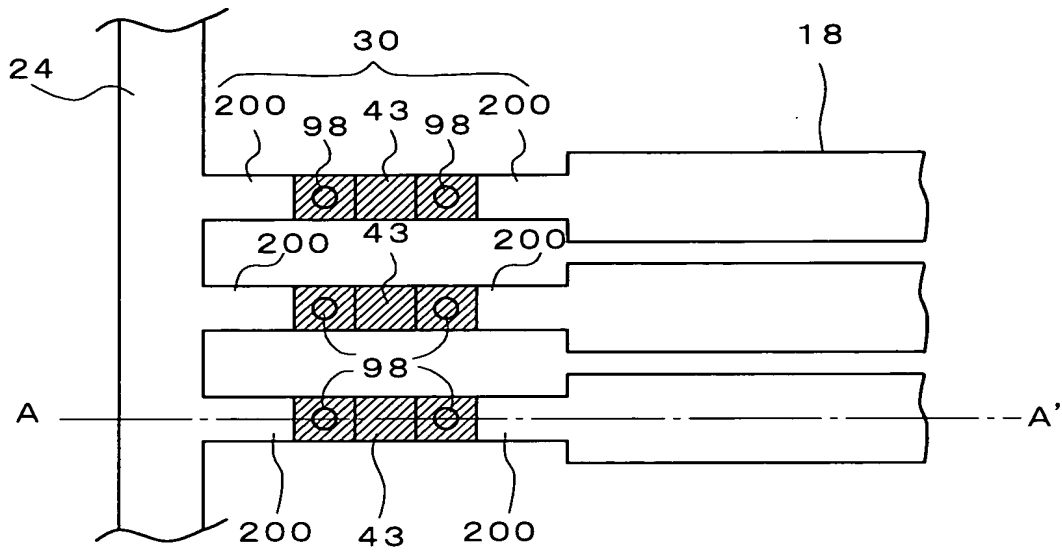


FIG. 23b

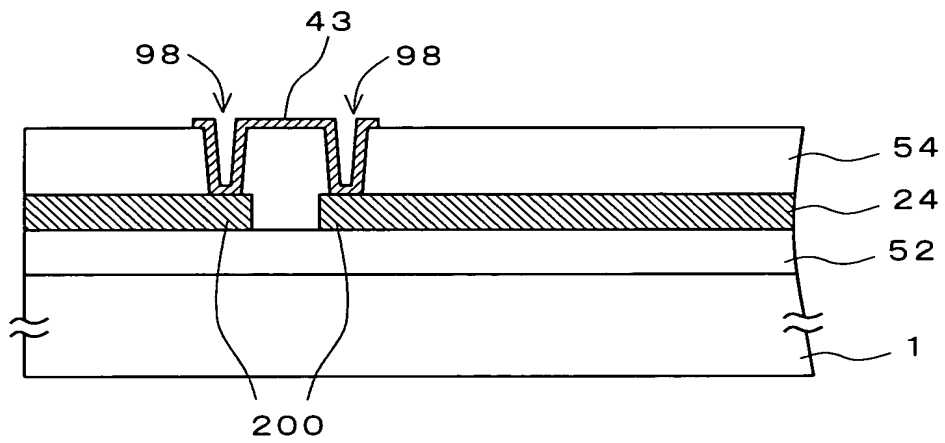


FIG. 24a

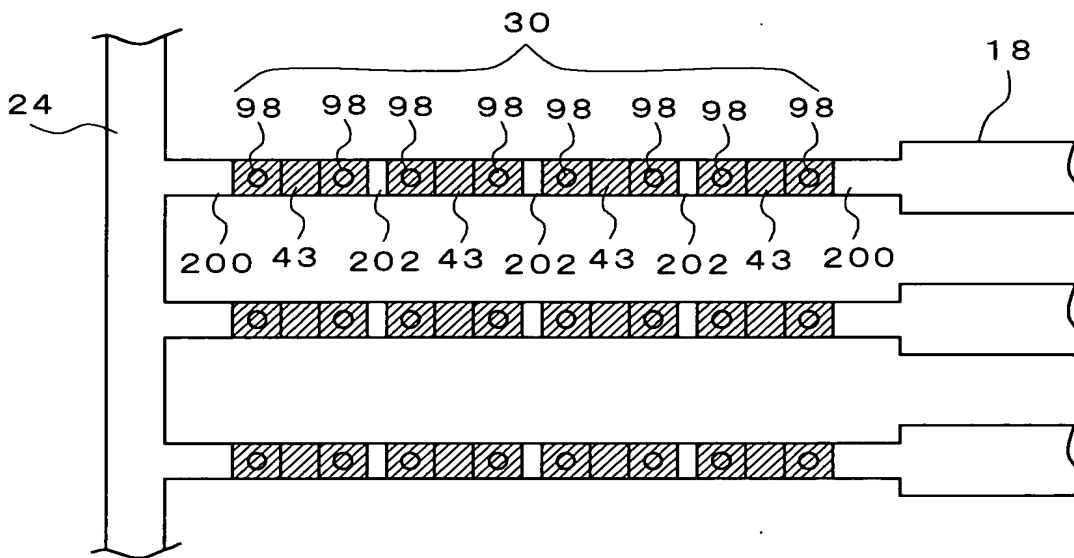


FIG. 24b

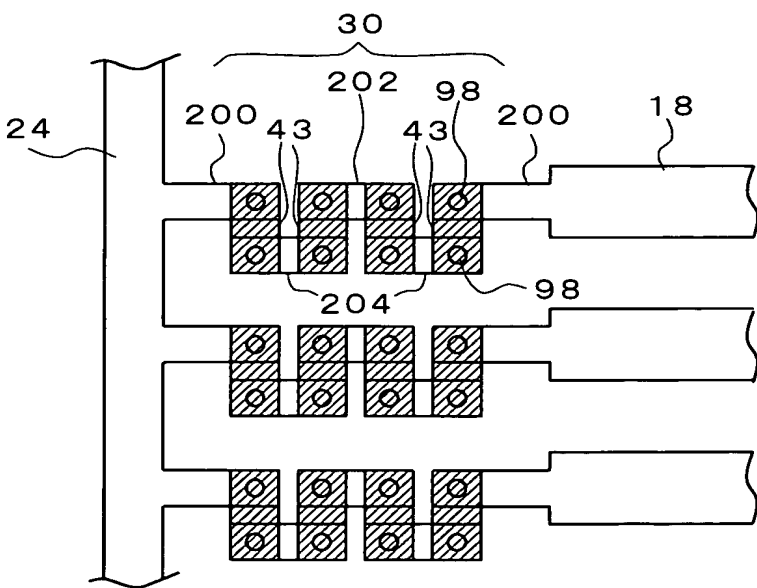


FIG. 25

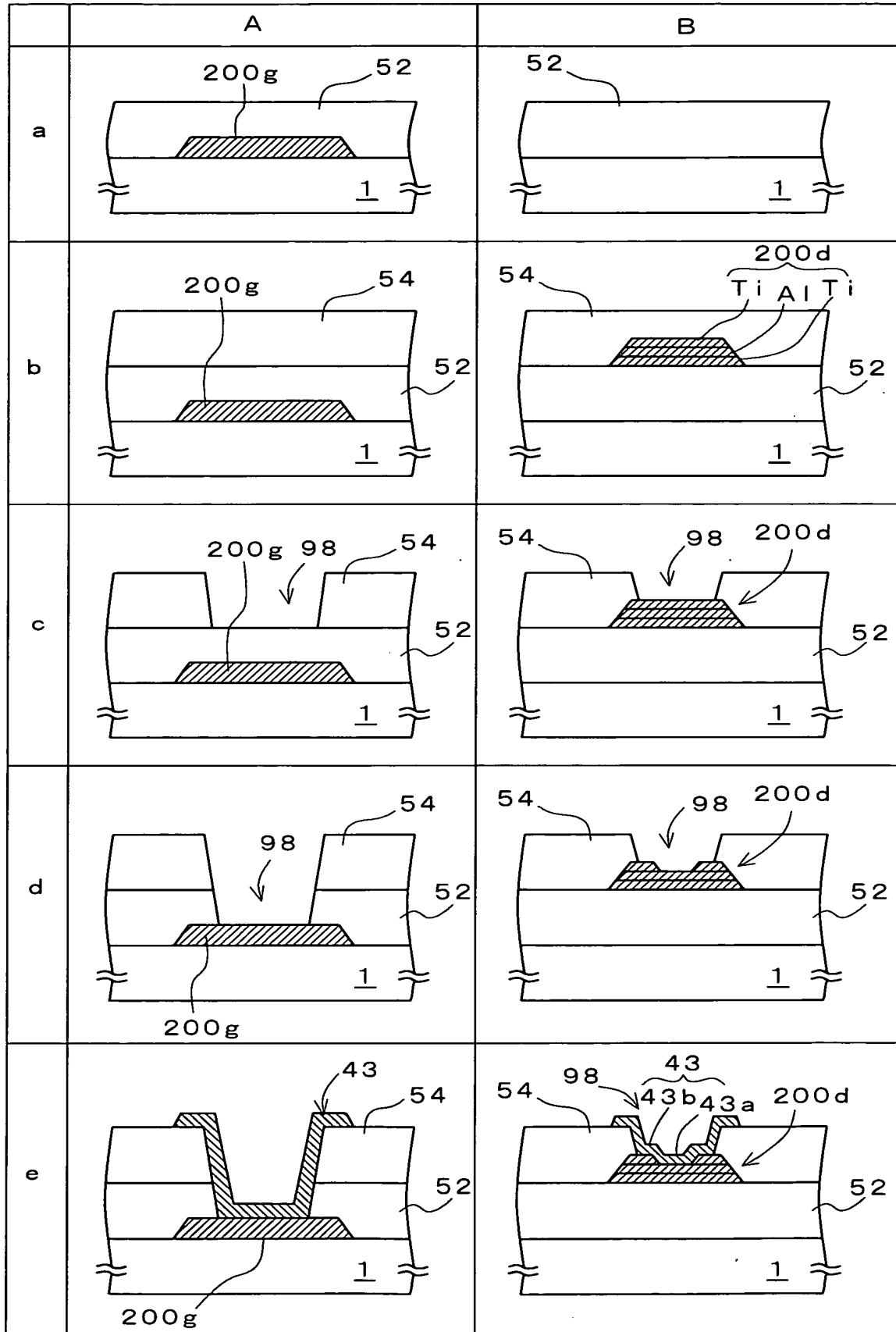
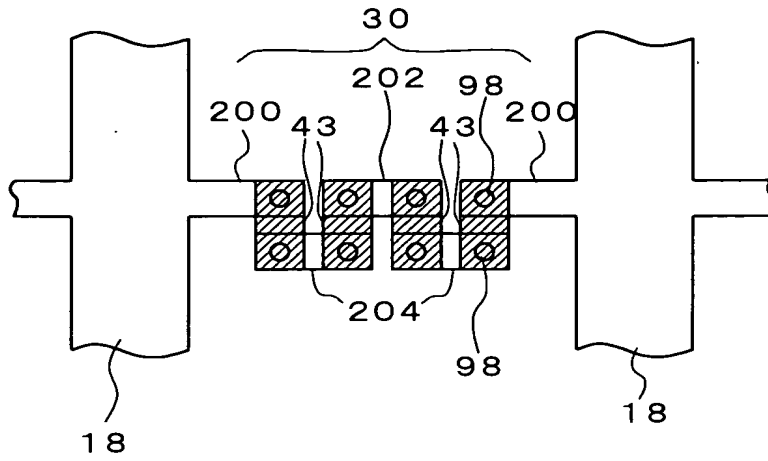
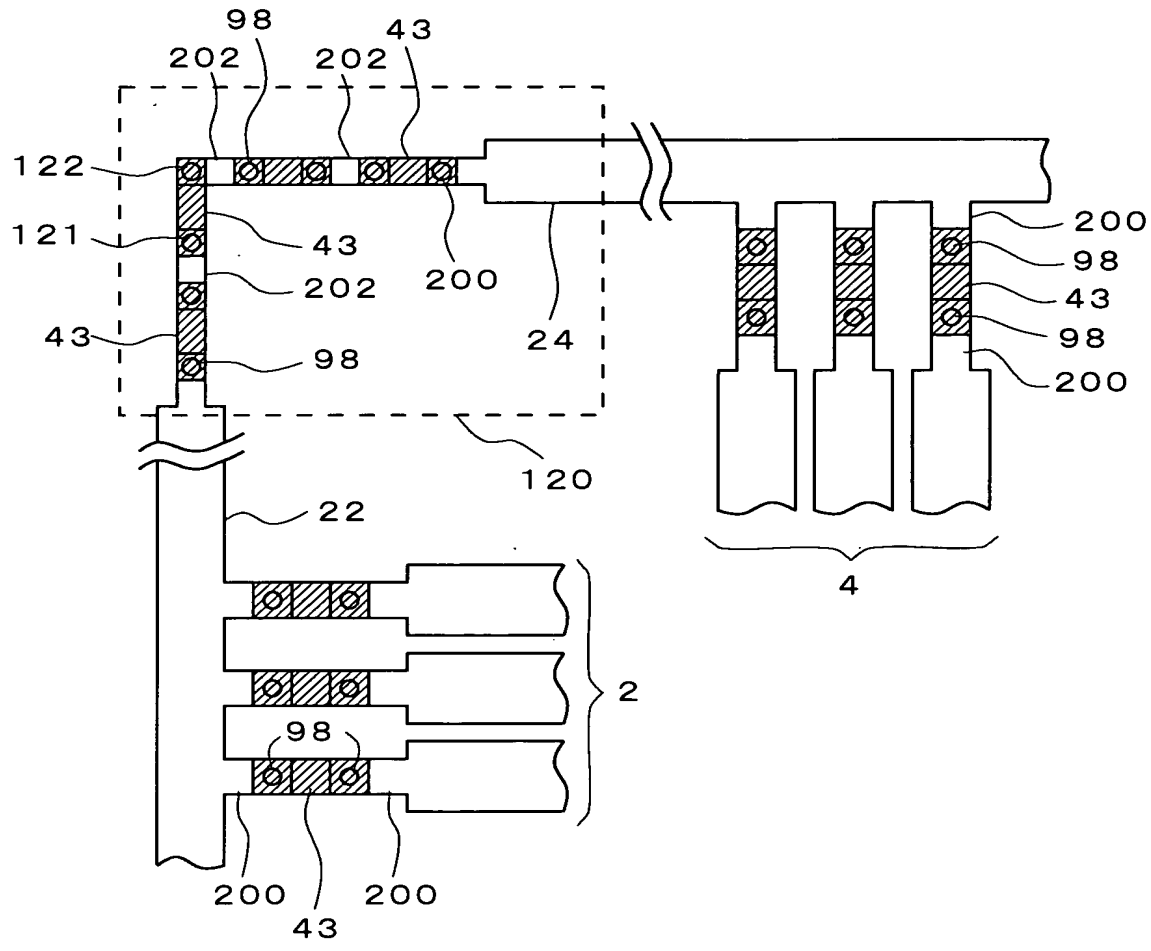


FIG. 26



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FIG. 27



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FIG. 28

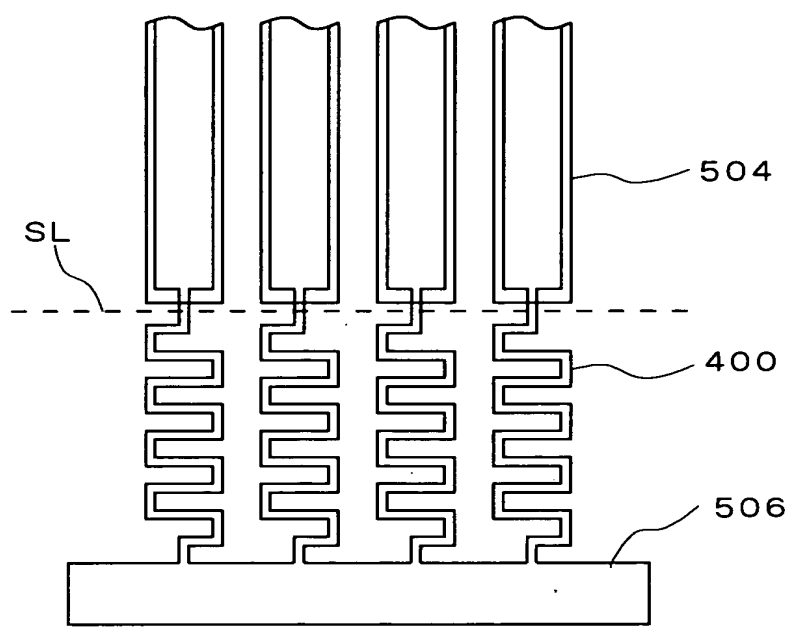


FIG. 29a

FIG. 29b

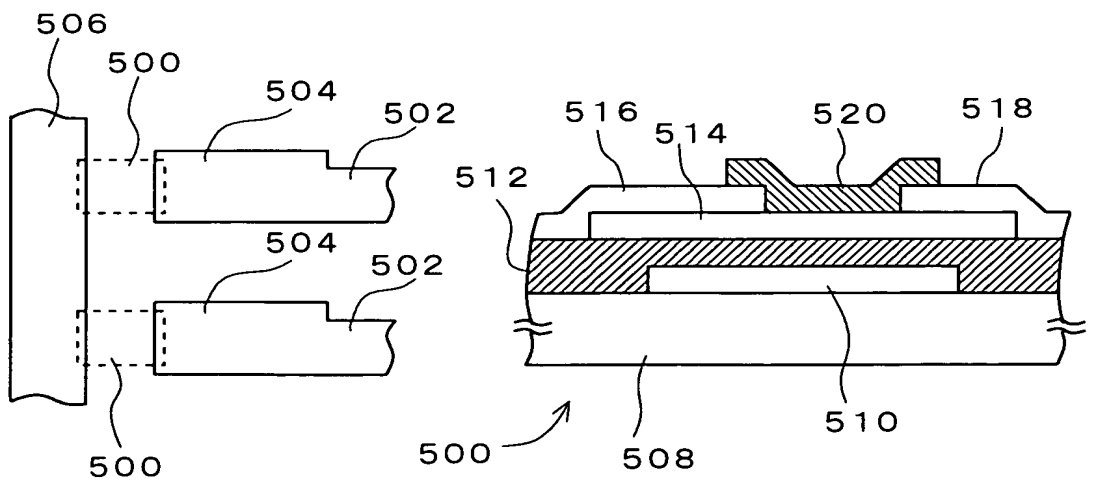
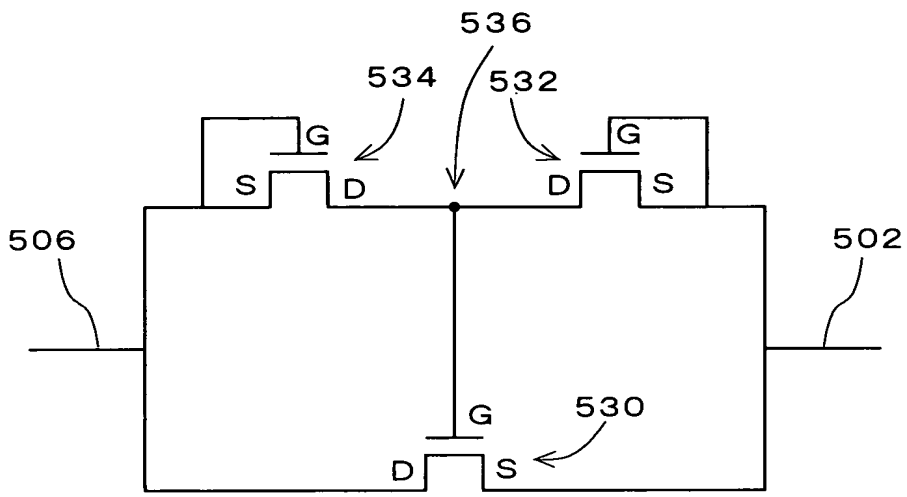


FIG. 30



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FIG. 31

